PTC/SB/08A (10-01)
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			-	First Named Inv nt r	Jason H. Anderson	
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		HALTER, JONATHAN P., "A Gate-Level Leakage Power Reduction Method for Ultra-Low-Power CMOS Circuits," IEEE Custom Integrated Circuits Conference, 1997, pages 475-478, IEEE, 3 Park Avenue, 17th Floor, New York, NY., 10016-5997.			
		YEAP, GARY, "Practical Low Power Digital VLSI Design," 1998, pages 59-72, available from Kluwer Academic Publishers, 101 Philip Drive, Assinippi Park, Norwell, Massachusetts, 02061			
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